	Aims and Objectives		
E 3.05 Digital System Design	 How to go about designing complex, <i>high speed</i> digital systems (not just circuits)? How to use some of the modern <i>CAD tools</i> to help with the design? How to implement such designs using <i>programmable logic</i> 		
Peter Cheung Department of Electrical & Electronic Engineering Imperial College London	 How to implement such designs using <i>programmable logic</i> (e.g. FPGAs)? How to read <i>data sheets</i> and make sense of them? How do <i>digital building blocks</i> (such as memory chips, processing elements, arithmetic circuits etc.) work? How to interface to processors and computers (from hardware point of view)? 		
URL: www.ee.ic.ac.uk/pcheung/ E-mail: p.cheung@ic.ac.uk	 How to deal with testing of complex systems? Have fun! 		
PYKC 3-Jan-08 E3.05 Digital System Design Topic 1 Slide 1	PYKC 3-Jan-08 E3.05 Digital System Design Topic 1 Slide 2		
Course Syllabus	Course Syllabus (1) – Programmable Logic		
 The course syllabus is divided into five main sections: Programmable Logic Arithmetic Circuits Data Encoding & communication Architectures 	 Technologies behind programmable logic Programmable Logic architectures in general Complex Programmable Logic Devices (CPLDs) Field Programmable Gate Arrays (FPGAs) 		

Testing

- ◆ Recent advances in FPGAs
- Designing with FPGAs
- Design Flow, Design Tools, Design Libraries
- Future of programmable logic

Topic 1 Slide 3

Course Syllabus (2) – Arithmetic Circuits	Course Syllabus (3) – Data Encoding & Communication		
 Adders architectures Multipliers circuits Floating point arithmetic circuits Other computational building blocks 	 Logic interface standards Clocking for high speed digital design Metastability issues Clock synchronisation Data encode and error correction On-chip and On-board communication 		
^r KC 3-Jan-08 Topic 1 Silde 5 Course Syllabus (4) – Hardware Architectures	PYKC 3-Jan-08 E3.05 Digital System Design Topic 1 Slide 6 Course Syllabus (5) – Digital Test		
 Parallel vs serial Systolic and other array architectures Distributed arithmetic Cordic based architecture 	 Modern packaging Board testing issues JTAG Boundary Scan 		
YKC 3-Jan-08 E3.05 Digital System Design Topic 1 Slide 7	PYKC 3-Jan-08 E3.05 Digital System Design Topic 1 Silde 8		

Recommended Books

Coursework

No perfect textbook for this course. Here are four reasonable possibilities:

- "Digital Design Principles and Practices", 4th Edition (Sept 2005), John F. Wakerly, Prentice Hall.
 - This is a new edition of a well established textbook. It covers a significant portion of the materials taught on this course. At ~£45, this a bargain. Recommended purchase if you have not already done so!
- "Contemporary Logic Design", Gaetano Boriello, Randy H. Katz, August 2004, Prentice Hall.
 - Good coverage on finite state machines and computer architectures. (~£45)
- "High-Speed Digital Design A handbook of black magic", Howard G. Johnson, Prentice Hall, 1993; ISBN 0-13-395724-1 (£61).
 - The best practical guide to designing and building very high speed digital circuits. Expensive reference for your company to buy (not you).
- "FPGA-based System Design", Wayne Wolf, Prentice Hall, 2004, ISBN 0131424610 (£75)
 - Contemporary book based on FPGA; possibly too expensive for what it covers

E3.05 Digital System Design

Topic 1 Slide 9

- Best way to learn DSD is to do it!
- Unassessed coursework:
 - 2 to 8 lab exercises using DE2 Board (from Altera) to learn the system
- Assessed coursework:
 - Design of a cordic based processor to add ripple effect on an image
 - Work in pairs one deliverable between the pair
- Deliverables:
 - Working design and demonstrator
 - Design document (effectively a no-nonsense report)
 - Deadline: 1st day of the Summer Term
- Quartus-II software has a web-edition that can be downloaded (free) from Altera website after you register
- Software also available on all Level 5 & Level 1 machines
- DE2 Boards available on Level 5 and Level 1 Labs

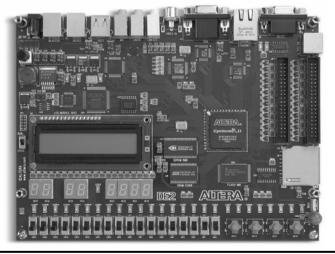
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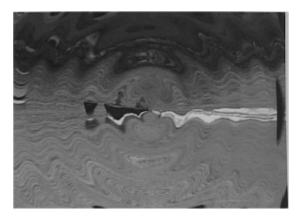
Coursework – DE2 Board

http://www.altera.com/education/univ/materials/boards/unv-de2-board.html



Coursework – Demo

 This shows an example of the ripple video effect which is the goal of this coursework



E3.05 Digital System Design

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Levels of Design Abstractions

Design Levels	Design Descriptions	Primitive Components	Theoretical Techniques
Algorithmic	Specifications	Functional blocks	Signal processing theory
	High-level lang.	'black boxes'	Control theory
	Math. equations		Sorting algorithm
Functional	VHDL, Verilog	Registers	Automata theory
	FSM language	Counters	Timing analysis
	C/Pascal	ALU	
Logic	Boolean equations	Logic gates	Boolean algebra
	Truth tables	Flip-flops	K-map
	Timing diagrams		Boolean minimization
Circuit	Circuit equations	Transistors	Linear/non-linear eq.
	Transistor netlist	Passive comp.	Fourier analysis

Topic 1

Design Methodologies & Implementation Technologies

Peter Cheung Department of Electrical & Electronic Engineering Imperial College London

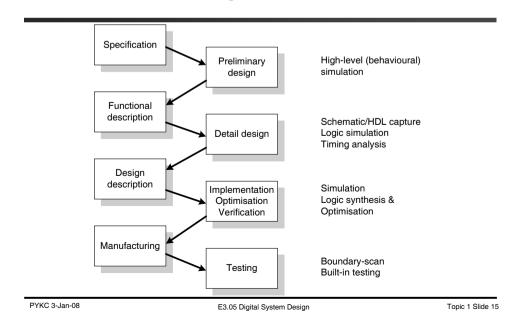
> URL: www.ee.imperial.ac.uk/pcheung/ E-mail: p.cheung@imperial.ac.uk

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The Design Process



The Design Process (cont')

Top-down design strategies

- Refine Specification successively
- Decompose each component into small components
- Lowest-level primitive components
- Over-sold methodology only works with plenty of experience

Bottom-up design strategies

- Build-up from primitive components
- Combined to form more complex components
- Risk wrong interpretation of specifications

Mixed strategies

- Mostly top-down, but also bits of bottom-up
- Reality: need to know both top level and bottom level constraints

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Ρ	Y٢	C	3	Jar	1-O	8

Design Descriptions

Design Tools

Schematic capture	Hardware Description Languages	Modern_dia	ital design systems contain the mo	ost of the followin
Good for multiple data flow Give overview picture Relates to hardware better Doesn't need to be good in computing High information density Back annotations possible Mixed analogue/digital possible	Flexible & parameterisable Excellent for optimisation & synthesi Direct mapping to algorithms Excellent for datapaths Readily interfaced to optimiser Easy to handle and transmit (electronically)	features: • Schematio • Hardwar I • Logic Synt • Timing An	Capture • Symbol Ed Description Language • Simulation thesis & Optimisation • Autoplace	diting n with Timing ment and Routing Editing
Not good for algorithms Not good for datapaths Doesn't interface well in optimiser No good for synthesis software Difficult to reuse Not parameterisable	Essentially serial representation May not show overall picture Often need good programming skill Divorce from physical hardware Need special software	• Hierarchic	al Design Management	
Jan-08 E3.05 [igital System Design	Topic 1 Slide 17 PYKC 3-Jan-08	E3.05 Digital System Design	Topic 1 S
A typical dig	ital system		mplementation Technol	ogies
A typical dig	ital system		mplementation Technol	ogies
	ital system M/ROM Buffer memo		Digital Logic	Full Custom
Microprocessor RA		ries Standard Lo	Digital Logic	Full Custom Microprocessor & RAM

ologies

